Short Papers

GaAs Monolithic Low-Power Amplifiers with *RC* Parallel Feedback

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Abstract — **GaAs monolithic broad-band low-power-dissipated amplifiers with inductive/resistive load and *RC* parallel feedback circuits have been developed. An inductive load amplifier provides a gain of 8 dB, a 3-dB bandwidth of 2.5 GHz, and a noise figure of 2.7 dB at 1 GHz with less than +1-V supply voltage and very low-power dissipation of 20 mW. A resistive load two-stage amplifier provides a gain of 15 dB and a 3-dB bandwidth of 2 GHz. Input and output reflection coefficients at 1 GHz are −13 dB and −21 dB, respectively.**

I. Introduction

Various types of GaAs monolithic microwave amplifiers have been developed in the last few years [1]–[5]. Although the direct coupled GaAs FET amplifiers reported by Van Tuyl [1] have very broad bandwidth in relation to their gain, they have neither good input/output matching nor a low noise figure. The amplifiers with a shunt resistor for negative feedback are capable of obtaining a broad bandwidth both for flat gain and for input and output matching [6]. A negative feedback GaAs FET amplifier having good input matching has been developed by using a feedback resistor and a depletion-type FET load [2]. In order to improve the bandwidth, noise figure, and power dissipation, we adopted an inductive/resistive load, which is used for dc voltage supply and RF choke, for negative feedback GaAs FET amplifiers.

In this work, inductive/resistive load GaAs broad-band monolithic amplifiers using negative feedback have been developed. They have low power dissipation and can be operated even with single dc supply voltage. Two types of amplifiers have been fabricated. They are a resistive load single-stage amplifier and a resistive load two-stage amplifier. These resistive load amplifiers can be operated as inductive load amplifiers. Performance characteristics of these amplifiers are described in detail with the discussion of the circuit design.

II. Design

Fig. 1 shows circuit diagrams of the two fabricated amplifiers, a resistive load single-stage amplifier and a resistive load two-stage amplifier. Resistive load amplifiers can be used as inductive load amplifiers as shown in Fig. 1(a), and can be operated with very low dc supply voltage.

Feedback resistance R_F is determined so as to minimize input and output reflection. The value of R_F depends mainly on the transconductance of the FET (g_m) and the source resistance R_s, and is determined by the approximate method [6].

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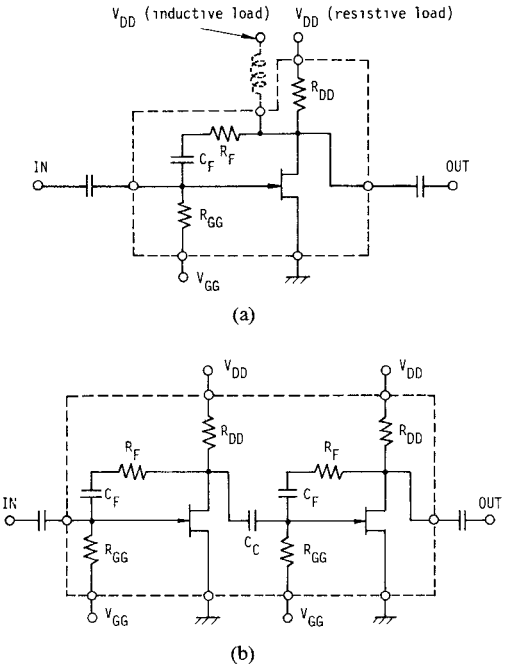

Fig. 1. Circuit schematics for MMIC amplifiers. (a) Single-stage amplifier. (b) Two-stage amplifier.

TABLE I
DESIGNED CIRCUIT PARAMETERS

R_{DD} and R_F	: 200 Ω
R_{GG}	: 2kΩ
C_C and C_F	: 20pF
gate length of FET:	1μm
gate width of FET :	1000μm

To determine the final circuit parameters for fabrication, the gain, input and output reflection coefficients, and input–output power response are calculated by using the circuit simulation program ASTAP. The GaAs MESFET device model described in [7] is used for the computer simulation. The parameters of the designed circuit are shown in Table I. The threshold voltage, saturation current at the gate–source voltage of 0 V and the transconductance of the FET used for the single dc-bias amplifier are −0.4 V, 20 mA, and 80 mS/mm, respectively. The gate–source capacitance, the gate–drain capacitance and the gate–source stray capacitance of the FET under the above conditions are 1.5, 0.12, and 0.05 pF, respectively.

III. Fabrication and Performance

A closely spaced electrode FET structure [8] is adopted for GaAs FET monolithic amplifiers. The source–gate and drain–gate spacings are both 0.4 μm, and the gate length is 1 μm. The gate width is 1000 μm. The active layers are formed by vapor phase epitaxy. The epitaxial layer has the impurity concentration of 1.9×10^{17} cm^{-3}. Gate metal is Al. AuGe-Ni was used to form the

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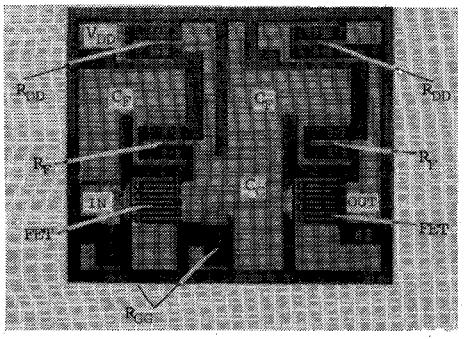

Fig. 2. A top view of the MMIC chip (the resistive load two-stage amplifier).

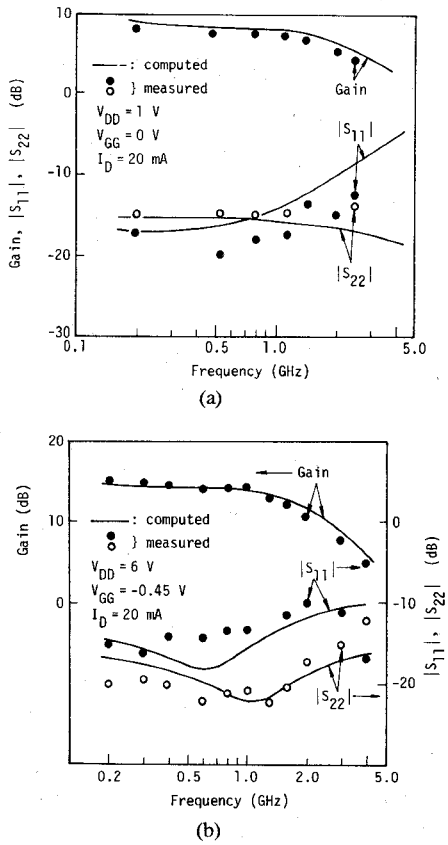

Fig. 3. Gain, $|S_{11}|$, and $|S_{22}|$ of the monolithic amplifiers. (a) Inductive load single-stage amplifier. (b) Resistive load two-stage amplifier.

ohmic contacts. The nonrecessed gate structure maintains uniformity for the epitaxial active layers.

A photomicrograph of the resistive load two-stage amplifier is shown in Fig. 2. The chip size is 1.0×1.4 mm^2.

The measured RF performance of a single-stage inductive load amplifier is shown in Fig. 3(a). A gain of 8 dB, a 3-dB bandwidth of 2.5 GHz, an input reflection coefficient of -17 dB, and an output reflection coefficient of -14 dB at 1 GHz are obtained with a single 1-V supply voltage. The power dissipation of this amplifier is only 20 mW. In this figure, the computed S-parameters are also shown, which are calculated considering the 0.5-nH inductances caused by bonding-wires and the 0.05-pF stray capacitances caused by input and output transmission lines. These computed values closely agree with the measured values.

Similar RF performance characteristics are obtained with a +6-V supply voltage and a 20-mA drain current when this amplifier is used as a resistive load amplifier.

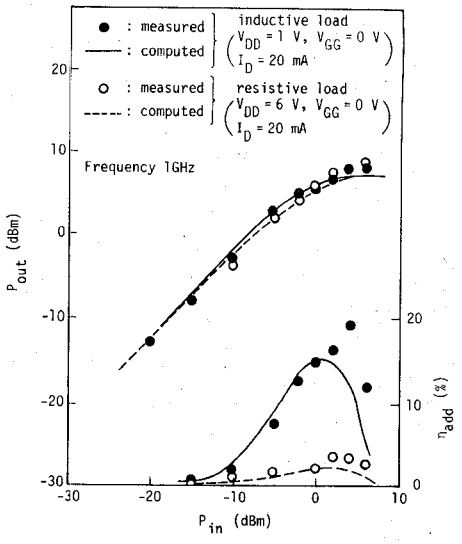

Fig. 4. Input–output power response of single-stage amplifiers.

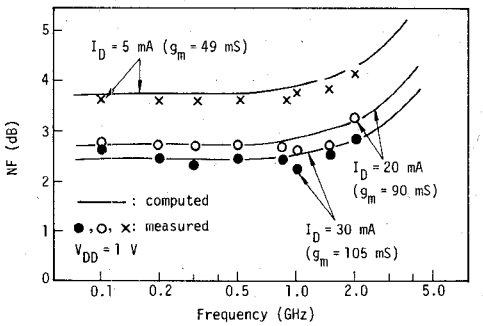

Fig. 5. Noise figure of the inductive load single-stage amplifier.

Fig. 3(b) shows the performance of a resistive load two-stage amplifier. The values of the circuit elements are the same as those of the one-stage amplifier mentioned above, except for the threshold voltage of about -0.75 V for the GaAs MESFET. A 3-dB bandwidth of 2 GHz is obtained with a gain of 15 dB under a power dissipation of 120 mW. $|S_{11}|$ and $|S_{22}|$ are -13 and -21 dB at 1 GHz, respectively.

The input–output power responses of the inductive and resistive load single-stage amplifiers are plotted in Fig. 4 with the power-added efficiency η_{add}. The maximum output power is 8 dBm for both the inductive load and resistive load. Power-added efficiency η_{add} exceeds 10 percent in the range of -4 dBm $< P_{in} < 6$ dBm, which is excellent for such a small-signal amplifier.

Fig. 5 shows the noise figure of the inductive load single-stage amplifier. Less than 2.8 dB is obtained over the whole frequency range of from 100 MHz to 2.2 GHz. The noise figures are calculated by the modified circuit simulation program SPICE for the fabricated GaAs amplifiers, assuming that $P = 2/3$, where P is the well-known factor in the expression for the drain-current noise defined by $i_{dn} = 4kT\Delta f g_m P$ [9]. The computed noise figures are in good agreement with the measured ones. These results indicate that the better the transconductance is, the smaller the noise figure becomes.

IV. Conclusion

GaAs monolithic FET amplifiers with a shunt feedback to provide good input and output matching and broad-band re-

sponse have been realized. The inductive load single-stage amplifier has a 3-dB bandwidth of 2.5 GHz, a gain of 8 dB, and a noise figure of 2.7 dB with a power dissipation of only 20 mW. Furthermore, it can be operated with single dc supply voltage. The resistive load two-stage amplifier has a 3-dB bandwidth of 2 GHz, a gain of 15 dB, and input and output reflection coefficients of -13 and -21 dB, respectively.

It is expected that these GaAs monolithic amplifiers will effectively improve the performance of UHF-band mobile communication equipment, especially for pocketable telephones. They will also be effective as IF amplifiers for satellite communication equipment.

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Tolerance Analysis of Shielded Microstrip Lines

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***Abstract*—A complete analysis of the sensitivities of shielded microstrips is presented. The sensitivity formulas form the basis for studying the effect of tolerances on the performance of these circuits. A set of sensitivity curves are given to help the design procedure. It is suggested that the position of the top cover can be adjusted to compensate for some of the effects of the manufacturing tolerances. Practical examples are given to support the suggested procedure.**

I. Introduction

A basic disadvantage of the microstrip circuits lies in the fact that their dimensions cannot be altered after manufacturing, so that the designer has to produce many circuits until he finds the circuit that meets the desired specifications.

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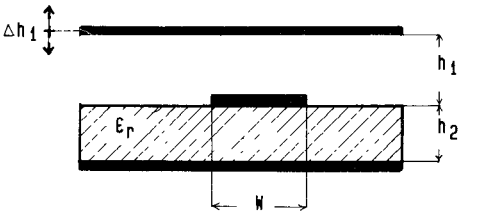

Fig. 1. Shielded microstrip structure with variable shield heights ratio.

In this paper, we suggest the shielded microstrip circuit shown in Fig. 1 with variable shield heights ratio, i.e., the position of the top cover may be changed to compensate for the effect of a given set of manufacturing tolerances. The designer may simply move the top cover up and down until the response of his designed circuit meets the desired specifications. As shown in earlier publications, microstrip parameters are influenced by the frequency f and strip thickness t, but they are mainly functions of the strip width W, substrate thickness h_2, value of the dielectric constant ϵ_r, and shield height h_1. Any changes in the values of W, h_2, ϵ_r, and h_1 give rise to corresponding changes in the microstrip parameters. In other words, any manufacturing tolerances in W, h_2, ϵ_r, and h_1 contribute to variations in the parameters of the shielded microstrip circuit.

II. Effect of Manufacturing Tolerances

The effect of tolerances on the performance of the shielded microstrip can be analyzed using the sensitivity approach [1], [2]. This is the easiest method of predicting the worst case for the change in Z_0 and the relative effective dielectric constant ϵ_{re}, corresponding to a set of tolerances. The change in the values of Z_0 and ϵ_{re} can be evaluated using the following relations:

$$\frac{\Delta Z_0}{Z_0} = \frac{\Delta W}{W} S_W^{Z_0} + \frac{\Delta h_2}{h_2} S_{h_2}^{Z_0} + \frac{\Delta \epsilon_r}{\epsilon_r} S_{\epsilon_r}^{Z_0} + \frac{\Delta h_1}{h_1} S_{h_1}^{Z_0} \quad (1a)$$

$$\frac{\Delta \epsilon_{re}}{\epsilon_{re}} = \frac{\Delta W}{W} S_W^{\epsilon_{re}} + \frac{\Delta h_2}{h_2} S_{h_2}^{\epsilon_{re}} + \frac{\Delta \epsilon_r}{\epsilon_r} S_{\epsilon_r}^{\epsilon_{re}} \rightarrow \frac{\Delta h_1}{h_1} S_{h_1}^{\epsilon_{re}} \quad (1b)$$

where W, h_2, ϵ_r, and h_1 are the tolerances in W, h_2, ϵ_r, and h_1, respectively, and the sensitivity S_B^A is defined as

$$S_B^A = \frac{B}{A} \frac{\partial A}{\partial B}. \quad (2)$$

A complete set of graphs for the sensitivities of Z_0 and ϵ_{re} with respect to W, h_2, ϵ_r, and h_1 ($S_W^{Z_0}$, $S_{h_2}^{Z_0}$, $S_{\epsilon_r}^{Z_0}$, $S_{h_1}^{Z_0}$, $S_W^{\epsilon_{re}}$, $S_{h_2}^{\epsilon_{re}}$, $S_{\epsilon_r}^{\epsilon_{re}}$, and $S_{h_1}^{\epsilon_{re}}$) as functions of the width to height ratio W/h_2 for $\epsilon_r = 9.6$ and at different shield heights ratios h_1/h_2 are given in Fig. 2(a) to 2(h). The most important facts that can be pointed out are listed below.

a) The sensitivity curves for Z_0 and ϵ_{re} are free from any discontinuities.

b) $S_W^{Z_0}$, $S_{\epsilon_r}^{Z_0}$, and $S_{h_2}^{\epsilon_{re}}$ are negative.

c) High-impedance shielded microstriplines ($W \leqslant h_2$) are more sensitive to tolerances in ϵ_r than tolerances in W, h_1, and h_2.

d) Low-impedance shielded microstriplines ($W \geqslant h_2$) are less sensitive to tolerances in ϵ_r than tolerances in W, h_1, and h_2.

e) For unity shield heights ratio $h_1/h_2 = 1$, the sensitivities $S_r^{Z_0}$, S_r^{re}, and S_W^{re} have the following values:

$$S_{\epsilon_r}^{Z_0} = -\epsilon_r/(2+2\epsilon_r) \quad (3a)$$

$$S_{\epsilon_r}^{\epsilon_{re}} = \epsilon_r/(1+\epsilon_r) \quad (3b)$$